ECE 271 – Introduction to Digital Circuits and Systems  
HW #4 - Due 11 February 2020

Note: this homework is TRICKY. Start early. If you get confused, draw yourself some timing diagrams – what does each element do, and why? And remember to look up the definitions of Tsetup, Thold, Clk->Q, and Metastability from class.

1.) The follow circuit has a delay of 1.0ns for all combinational gates. Tsetup is 0.5, Clk->Q is 0.25, Thold is 0.75.
   a.) What is the smallest legal clock period for this circuit?
   b.) What is the largest legal Thold, assuming the other parameters stay the same?

![Circuit Diagram]

2.) For the following circuits, assume Tsetup and Thold are 0.1ns, Clk->Q is 1.0 ns, all gate delays are 1.0ns, and the clock period is 100ns. “In” is an external input to the circuit, and all DFFs were initialized to 0 before the circuit started running. For each circuit, figure out whether OUT can ever be a 1. If it can, give a specific scenario when this can happen. If it cannot, explain why.

A.)

B.)

C.)

D.)