Registers

- Readings: 5.8-5.9.3
- Storage unit. Can hold an n-bit value
- Composed of a group of n flip-flops
  - Each flip-flop stores 1 bit of information

![Diagram of flip-flops]

\[ D \quad Q \]
\[ \text{Dff} \quad \text{clk} \]
\[ D \quad Q \]
\[ \text{Dff} \quad \text{clk} \]
\[ D \quad Q \]
\[ \text{Dff} \quad \text{clk} \]
\[ D \quad Q \]
\[ \text{Dff} \quad \text{clk} \]
# Controlled Register

<table>
<thead>
<tr>
<th>Reset</th>
<th>Load</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q = old Q</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Q = 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Q = D</td>
</tr>
</tbody>
</table>

- **D**
- **Q**

![DFF Diagrams]

179
Shift Register

- Register that shifts the binary values in one or both directions
Transfer of Data

- 2 modes of communication: Parallel vs. Serial
  - Parallel: all bits transferred at the same time
  - Serial: one bit transferred at a time
- Shift register can be used for serial transfer
### Shift Register w/Parallel Load

<table>
<thead>
<tr>
<th>Shift</th>
<th>Load</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q = old Q</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Shift</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>Parallel Load</td>
</tr>
</tbody>
</table>

![Diagram of D flip-flops with clock inputs](image-url)
## Conversion between Parallel & Serial

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Op - Sender</th>
<th>Q0</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Op - Recvr</th>
<th>Q0</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
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<td></td>
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<td>2</td>
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<tr>
<td>3</td>
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<tr>
<td>5</td>
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<tr>
<td>6</td>
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<tr>
<td>7</td>
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<tr>
<td>8</td>
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<td>9</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Bidirectional Shift Register w/Parallel Load

<table>
<thead>
<tr>
<th>Shift</th>
<th>Load</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q = old Q</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Parallel Load</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Shift Up (V*2)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Shift Down (V/2)</td>
</tr>
</tbody>
</table>

![Diagram of D flip-flop with clock (clk), input (D), and output (Q)](image-url)
Counters

- A reg. that goes through a specific state sequence
- *n-bit Binary Counter*: counts from 0 to $2^N - 1$ in binary
- *Up Counter*: Binary value increases by 1
- *Down Counter*: Binary value decreases by 1
- 3-bit binary up counter state diagram:
Binary Up-Counter Imp.
## Complex Binary Counter

<table>
<thead>
<tr>
<th>Load</th>
<th>Count</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q = old Q</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Up Count</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Reset</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Load Parallel</td>
</tr>
</tbody>
</table>
Arbitrary Sequence Counters

- Design a 3-bit count that goes through the sequence 000->010->100->101->111->110->001->011->000->...
Counters in Verilog

module upcounter #(parameter WIDTH=8)
  (out, incr, reset, clk);

  output logic [WIDTH-1:0] out;
  input logic incr, reset, clk;

endmodule
Memory

- Need method for storing large amounts of data
  - Computer programs, data, pictures, etc.

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000</td>
<td>00111110</td>
</tr>
<tr>
<td>000001</td>
<td>01101011</td>
</tr>
<tr>
<td>000010</td>
<td>01011101</td>
</tr>
<tr>
<td>000011</td>
<td>01100011</td>
</tr>
<tr>
<td>000100</td>
<td>00111110</td>
</tr>
<tr>
<td>000101</td>
<td>00000000</td>
</tr>
<tr>
<td>000110</td>
<td>11111111</td>
</tr>
<tr>
<td>000111</td>
<td>01010101</td>
</tr>
<tr>
<td>001000</td>
<td>10101010</td>
</tr>
<tr>
<td>001001</td>
<td>00100001</td>
</tr>
<tr>
<td>001010</td>
<td>11011010</td>
</tr>
</tbody>
</table>

- RAM: Random Access Memory, Read/Write
- ROM: Read-only Memory
RAM Cell

- Requirements:
  - Store one bit of data
  - Change data based on input when row is selected

Input | D | Q
-----|---|---
Row Select | en
8x4 RAM

<table>
<thead>
<tr>
<th>Write</th>
<th>In3</th>
<th>In2</th>
<th>In1</th>
<th>In0</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>011</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>111</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3:8 Decoder</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A2 A1 A0  Out3  Out2  Out1  Out0
RAM example

- Use a memory to do a programmable 32-picture animation on a 7-segment display
module memory16x6 (data_out, data_in, addr, we, clk);

output logic [5:0] data_out;
input logic [5:0] data_in;
input logic [3:0] addr;
input logic we, clk;

logic [5:0] mem [15:0];

always_ff @(posedge clk) begin
  data_out <= mem[addr];
  if (we)
    mem[addr] <= data_in;
end

endmodule
Field Programmable Gate Arrays (FPGAs)

- Readings: B.6-B.6.5

Logic cells imbedded in a general routing structure

Logic cells usually contain:

- 6-input Boolean function calculator
- Flip-flop (1-bit memory)

All features electronically (re)programmable
Using an FPGA

Verilog

FPGA CAD Tools

Bitstream

Simulation

Verilog code for 2-input multiplexer

module AOI (F, A, B, C, D);
output F;
input A, B, C, D;
assign F = ~(A & B) | (~C & D);
endmodule

module MUX2 (V, SEL, I, J);
output V;
input SEL, I, J;
wire SELB, VB;
not G1 (SELB, SEL);
AOI G2 (VB, I, SEL, SELB, J);
not G3 (V, VB);
endmodule
FPGA Programming

Bitstream

\( \mathcal{P} = 1 \) memory cell (stores 1 bit of info)
FPGA Combinational Logic

- How can we use Muxes and Programming bits to compute combinational binary function $F(A,B,C)$?

- Creates a "LUT" or lookup table.
FPGA Sequential Logic

- How do we put DFF’s onto LUT outputs only when we need them?

- Creates a “LE” or logic block
FPGA Local Routing

- How do we combine LE’s to build larger functions?

In1

In2

In3

In4

- This is an Altera “LAB”.
FPGA Global Routing

- Can’t do all-to-all/crossbar routing, so what?
FPGA CAD

- CAD = “Computer-Aided Design”

- Tech Mapping: Convert Verilog to LUTs
- Placement: Assign LUTs to specific locations
- Routing: Wire inputs to outputs
- Bitstream Generation: Convert mapping to bits

Verilog

FPGA

CAD

Tools

Bitstream
Modern FPGA: Stratix V

- Logic Blocks
- Multipliers & DSP
- Embedded Memories
- Clocking Logic
- I/O Protocols
DE1-SoC FPGA: Cyclone V 5CSEMA5F31C6N

- ALMs (2x6-LUT): 32k
- DFFs: 128k
- RAMs (10Kb): 3.9k
- 18x18 Hard Multipliers: 174
- Clock generators (PLLs): 6
- General-purpose I/Os: 288
- ARM Cortex A9 cores: 2