Review Problem 23

- The following two flip-flops are subtly different, but both useful. The difference in code is shown in bold. What is the difference in their behavior?

```plaintext
module D_FF1 (q, d, reset, clk);
  output logic q;
  input logic d, reset, clk;

  always_ff @(posedge clk) begin
    if (reset)
      q <= 0;
    else
      q <= d;
  end

endmodule
```

```plaintext
module D_FF2 (q, d, reset, clk);
  output logic q;
  input logic d, reset, clk;

  always_ff @(posedge clk or posedge reset) begin
    if (reset)
      q <= 0;
    else
      q <= d;
  end

endmodule
```

Synchronous Reset

Asynchronous Reset
Subdividing FSMs

- Some problems best solved with multiple pieces

- Psychic Tester:
  - Machine generates pattern of 4 values (on or off)
  - If user guesses 8 patterns in a row, they’re psychic

- States?

  0 - 7 correct guesses (8)

  16 patterns
  128 states

Found a Psychic
Subdividing FSMs (cont.)

- Pieces?

Next pattern

Pick a pattern
(16 state FSM)

Count correct guesses
(8x9 state FSM)

Right?

Check guess

Use Input
(4 switches
1 "go" button)

Go

It's psyche
Flipflop Realities 1: Gating the Clock

D flipflop

D  Q

Clk

Clock  C

Enable

Enable

Clock

C

★ NEVER put a logic gate between the clock and DFF's CLK input.
Flipflop Realities 2: Clock Period, Applying Stimulus

- Clock Period?
- Apply Inputs when?

Clock

Diagram showing the relationship between inputs, clock, and flipflops, with labeled steps for input processing and clock synchronization.
\( T_{\text{setup}}, T_{\text{hold}}, \text{Clk} \rightarrow Q \)

- Flipflops require their inputs be stable for time period around clock edge

\[ \text{D} \quad \text{Can Change} \quad \text{Stable} \quad \text{Can Change} \]

\[ \text{Clock} \quad T_{\text{setup}} \quad T_{\text{hold}} \quad \text{Clk} \rightarrow Q \]

\[ \text{Q} \quad \text{Old Value} \quad \text{New Value} \]

Clock period \( \geq \text{Clk} \rightarrow Q + \text{State delays} + T_{\text{setup}} \).
Timing Definitions

- $T_{\text{setup}}$: Time D must be stable BEFORE clock edge
  - Often adds to critical path delay

- $\text{Clk} \rightarrow Q$: Time from clock edge to Q changing
  - Often adds to critical path delay

- $T_{\text{hold}}$: Time D must be stable AFTER clock edge
  - Can get violated by paths that are too short
Flipflop Realities 3: External Inputs

- External inputs aren’t synchronized to the clock

D __________
Clk __________
Q __________

Metastability: input transition within $T_{\text{setup}}..T_{\text{hold}}$ period causes DFF to strange middle value.

Behavior sketch:
- after Clk->Q the Q output goes to $\frac{1}{2}$
- stays there for ~1-2ns
- then randomly goes to 0 or 1
Dealing with Metastability

- Single DFF
  - Metastable

- 2 DFFs in series
  - Clean

- 2 DFFs in parallel
  - Clean