Assuming all gates have the same delay (including inverters), complete the following timing diagram.

Review Problem 9
Circuit can temporarily go to incorrect states

Hazards/Glitches
(re)programmable

All features electronically

Flip-flop (1-bit memory)

• Calculator
• 6-input Boolean function

Logic cells usually contain:

□

General routing structure

Logic cells imbedded in a

Field Programmable Gate Arrays (FPGA)
Using an FPGA
Superset of previous; cleaner and more efficient

Modern version is "System Verilog"

- VHDL similar to ADA
- Similar to C/C++/Java
- Enable tools to automatically create implementation
- Find bugs early
- Simulate behavior before (wasting time) implementing
- Programming language for describing hardware
module A01 (F, A, B, C, D);
// input logic A, B, C, D;
// output logic F;
assign F = ~(A & B) | (C & D);
endmodule

// end of Verilog code

// Comment

Structure Verilog

AND-OR-INVERT

Dont use +,
module AOI (F, A, B, C, D);

output F;
logic AB, CD, 0, inputs;
logic A, B, C, D;

assign F = ~0;
assign 0 = AB | CD;
assign CD = C & D;
assign AB = A & B;

endmodule

// Assign code for AND-OR-INVERT gate

Verilog Wires/Variables
Verilog code for AND-OR-INVERT gate

```
module some_module

    input logic A, B, C, D;
    output logic F;

    assign F = ~A & B | C & D;

endmodule
```

Verilog Gate Level