endmodule

default: teqs = 7'b1:

endcase

1111 (fifteen).

A on input pattern 1010 (ten) and F on pattern

Extend this Verilog code to also show the letter

Review Problem 19
True if an odd number of inputs are true

EX: Debug a 9-input odd parity circuit

Complex circuits require careful debugging
Debbuging Complex Circuits (cont.)
DO NOT RIP UP DEBUG!

- Look at values at intermediate points in circuit.
- Typically, trace backwords from bad outputs, forward from inputs.
- Value is wrong.
- Examine inputs and outputs to find earliest place where
- Identify any incorrect behaviors.
- All combinations of inputs for small circuits, subcircuits.
- Test all behaviors.

Debugging Approach
Combination vs. Sequential Logic

Readings: 5-5.4.4

Combinational Logic

- No feedback among inputs and outputs
- Outputs are a pure function of the inputs
- Distinctions between sequential and combinational networks
- The presence of feedback Network implemented from logic gates

Seat Belt Light

(Deploy, Pbelt, Passenger) mapped into (Light)

Combinational Logic

Network Logic

$X_1$ $X_2$ $X_{mn}$

Feedback

Combination Logic

$Z_1$ $Z_2$ $Z_m$
Must filter out temporary states

Circuit can temporarily go to incorrect states

Hazards/Glitches
Locked elements hide glitches/hazards

Clock signal synchronizes operation

Clock elements on feedback, perhaps outputs

Safe Sequential Circuits
module D Flip Flop

endmodule

always_ff @ (posedge clk)
begin
  q <= d;
end

endmodule