most TRUEs on the output

What is the series of inputs that will produce the

Review Problem 25
Circuit Diagram of FSM
end

forever # (clock_period/2) clk &~ clk:
  if clk &~ clk = 0:
    int test begin

    parameter clock_period=100;
    // Set up the clock.
    // Sample dut (clk, reset, w, out);
    logic clk, reset, w, out;

    module simple_testbench();

    FSM Testbench
endmodule // End the simulation.

$end

initital begin

FSM Testbench (cont.)

// ONLY USE THIS FORM FOR testbench!!!

Design inputs: Each time is a clock cycle. //
State Machine

Input: 1 0 1 0 1 0 1 0 1
Output: 1 0 1 0 1 0 1 0 1

Recognize the string: 101

String Recognizer Example
String Recognizer Example (cont.)

State Table:
String Recognizer Example (cont.)

Implementation
not including current input
any order, not necessarily consecutively (have been seen,
outputs a true once at least two 0's and at least two 1's (in
Draw the state diagram of a machine that continuously

Review Problem 29
Initail reset counts as a SD
0. FL to G, fire gray flame until the next SI

A busy highway is intersected by a little used farmland. Detectors

FSM Word Problem: Traffic Light Controller

Clock = 1 Hz
Picture of Highway/Farmroad Intersection:

Traffic Light Controller (cont.)
Start timing a short or long interval
assert green/yellow/redFarmroad lights
assert green/yellow/red Highway lights

Description

Long time interval expired
Short time interval expired
Detect vehicle on Farmroad
Place FSM in initial state

Table of Inputs and Outputs:

Traffic Light Controller (cont.)
Traffic Light Controller (cont.)

State Diagram

Note: Will only list four outputs.