Represent that number in 2's Complement.
What's the smallest number of bits required to represent that number?

Comment:
How would it be represented in 10-bit 2's Complement number (111010)?

Review Problem 41
Programmable for arbitrary functions

Elements for interconnections

**FPGA**

Multiple/Demultiplexer/Encoder/Decoder: Standard Routing

Single chip that performs very complex computations

Alternative: Complex chips for standard functions

Requires numerous chips to build interesting circuits

1 chip = 2-8 gates

Standard TTL Small-Scale Integration

Readings: 2.8-2.8.2

Basic Circuit Elements
Put together a simple telephone system

Design Example: Basic Telephone System
Operator controls all connections.

* Multiple subscribers, one operator.

Basic Telephone System (cont.)
Decoder: Convert binary to one-of-N wires
Encoder: Determine which input is active
Multiplexer: Combine N sources onto 1 wire
Used in Networks, Computers, Stereos, etc.

Blocks
Develop Implementations of Important Building
Standard Circuit Elements
Example: 3-to-8 decoder

A decoder that has \( n \) inputs and \( m \) outputs is referred to as

- \( n \times m \) or \( N:W \), where \( N \) is the number of inputs and \( W \) is the number of outputs

Input: \( N \) bits; output: \( 2^N \) outputs

Used to select one of \( 2^N \) outputs based on \( N \) input bits

Decoders
There are 9 inputs and 3 outputs.

Decoder Implementation

\[
\begin{array}{c|cccc|cc}
D_0 & D_1 & D_2 & D_3 & S_0 & S_1 \\
\hline
0 & 0 & 0 & 0 & 1 & 1 \\
0 & 0 & 0 & 1 & 0 & 1 \\
0 & 0 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 \\
\end{array}
\]
<table>
<thead>
<tr>
<th>En</th>
<th>S1</th>
<th>S0</th>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Active High enable

Enabled Decoder Implementation
module

else
endcase

end

endmodule

always_comb begin

endmodule

module decoder2_4 (out, in, enable);

parameter

input [3:0] in;

input [1:0] enable;

output [3:0] out;

endmodule

Endblad Decoders in Verilog
Construct a 4:16 decoder using 2:4 decoders