other gates as possible.

Build a full adder using 3:8 Decoders and as few gates as possible.

Review Problem 44
Multiplexer often abbreviated as MUX

Output: The data from one selected input line
Input: 2^n input lines and N selection lines

An element that selects data from one of many sources.
Turn off all non-active inputs:

\[ S_0 = 0 \]
\[ S_1 = 1 \]

\[ D_3 \quad 1 \quad 1 \\
D_2 \quad 0 \quad 1 \\
D_1 \quad 1 \quad 0 \\
D_0 \quad 0 \quad 0 \\
\]

\[ F = D_0 \cdot S_0 + D_1 S_1 S_0 + D_2 S_1 + D_3 S_1 S_0 \]

**4:1 MUX Multiplexer Implementation**
Construct a 16:1 MUX using 4:1 MUX's

Multiplexer Expansion
Implement $F = XYZ + X'Y'Z$ with an 8:1 MUX.
Implement $F = XYZ + X'Z'$ with a 4:1 MUX.

Multiplexers in General Logic (cont.)
Registers

- Readings: 5.4-5.5.1, 5.6.2
- Storage unit. Can hold an n-bit value
- Composed of a group of n flip-flops
- Each flip-flop stores 1 bit of information
Controlled Register

<table>
<thead>
<tr>
<th>D</th>
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<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Reset Load Action