Design the circuit for this output.

Assumption that only one input is true is not met.

Invalid which is true when the encoder's basic 4:2 encoder. However, we want an output instead of a priority encoder, we plan to use the
Multiplexer often abbreviated as MUX

Output: the data from one selected input line

Input: 2^N input lines and N selection lines

An element that selects data from one of many
**4:1 MUX**

Multiplexer Implementation

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>S0</td>
<td>F</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ F = \overline{S_1} \overline{S_0} D_0 + \overline{S_1} S_0 D_1 + S_1 \overline{S_0} D_2 + S_1 S_0 D_3 \]
Implement $F = \overline{XZ} + \overline{YZ}$ with an 8:1 MUX
Implementation of a 4:1 MUX with \[ XYZ + \overline{YZ} = \overline{X}Y \bar{Z} \] (cont.)
Each flip-flop stores 1 bit of information.

Composed of a group of n flip-flops.

Storage unit can hold an n-bit value.

Readings: 5.8-5.9.3

Registers
Controlled Register

\[
\begin{array}{c|c|c}
\text{Action} & \text{Load} & \text{Reset} \\
\hline
\text{A} = 0 & 1 & 0 \\
0 = 0 & \times & 1 \\
\hat{O} = 0 = 0 & 0 & 0 \\
\end{array}
\]
Shift Register

Register that shifts the binary values in one or both directions.

Clock