animation on a 7-segment display
Use a memory to do a programmable 32-picture

RAM example

Review Question
endmodule

eend

if (we)
data_out <= mem[addr]
always @ (posedge clk) begin

logic [15:0] mem [15:0]

logic [15:0] mem [15:0]

logic [3:0] addr;
logic [5:0] data_in;
logic [5:0] data_out;

module memory16x6 (data_in, data_out, addr, we, clk);

Verilog Memories
(re)programmable
All features electronically
- Flip-flop (1-bit memory)
- Calculator
- 6-input Boolean function

Logic cells usually contain:

General routing structure
Logic cells imbedded in a

Field Programmable Gate Arrays (FPGAs)

Readings: B.6-B.6.5
Simulation

Bistream

Tools

Verilog

Using an FPGA
$P = 1$ memory cell (stores 1 bit of info)
Create a "LUT" or Lookup table.

compute combinatorial function $F(A, B, C)$?

How can we use Muxes and Programming bits to FPGA Combinatorial Logic
When we need them?

How do we put DFF's onto LUT outputs only

FPGA Sequential Logic
This is an Altera "LAB".

How do we combine LE's to build larger functions?

FPGA Local Routing

Crossbar 4:1-16:1 - All Reach

20Q
Can't do all-to-all/crossbar routing, so what?
Bistream Generation: Convert mapping to bits
Routing: Wire inputs to outputs
Placement: Assign LUTs to specific locations
Tech Mapping: Convert Verilog to LUTs

FPGA = "Computer-Aided Design"

FPGA CAD
Modern FPGA: Stratix V

I/O Protocols
Clocking Logic
Embedded Memories
Multiplexers & DSP
Logic Blocks
ARM Cortex A9 cores: 2
General-Purpose I/Os: 288
Clock Generators (PLLs): 6
18x18 Hard Multipliers: 174
RAMs (10KB): 3.9K
DEFs: 128K
ALMs (2x6-LUT): 32K

DE1-SoC FPGA: Cyclone V Scemaster31CN