Review Problem 53

- If we only had 8x2 memories available, how could we make an 8x6 RAM?
(re)programmable
All features electrically
• Flip-flop (1-bit memory)
• Calculator
• 6-input Boolean function
Logic cells usually contain:

General routing structure
Logic cells imbedded in a

Field Programmable Gate Arrays (FPGAs)
FPGA Programming

$q = 1$ memory cell (stores 1 bit of info)
Create a "LUT" or lookup table.

- S-Input LUTs
- 6-Input LUTs
- Comb. A/LUT

How can we use Mixes and Programming bits to compute combinational binary function \( F(A, B, C) \)?

FPGA Combinational Logic
Creates a "LE" or Logic block

- How do we put DEFS onto LUT outputs only?
- When we need them?

FPGA Sequential Logic
This is an Altera "LAB"

How do we combine LE's to build larger circuits?

FPGA Local Routing

Out1

Out2

In1

In2

In3

In4

Functions

Allen is in (x,y, z) 100

Corner: start any input to any output

One step: check each input to each output

This circuit looks any input to any output
Can’t do all-to-all/crossbar routing, so what?

FPGA Global Routing
Bistream Generation: Convert mapping to bits
Routing: Wire inputs to outputs
Placement: Assign LUTs to specific locations
Tech Mapping: Convert Verilog to LUTs

FPGA CAD = "Computer-Aided Design"
DE1-SOC FPGA: Cyclone V 5CSMA5F31C6N

- ARM Cortex A9 cores: 2
- Clock generators (PLLs): 6
- General-purpose I/Os: 288
- 18x18 Hard Multipliers: 174
- RAMs (10Kb): 3.9k
- DFFs: 128k
- ALMs (2x6-LUT): 32k