What components are on your DE1-Soc board?

and how are they connected?
Advanced Verilog - Synthesis Optimizations
Advanced Verilog - Generate Statements

module adder #parameter WIDTH=3 (sum, overflow, a, b, cin);

assign overflow = carries[WIDTH-1] & carries[WIDTH-2];
assign cin[0] = cin;
endmodule

forall (t=0 : t<WIDTH ; t++) begin
  Q[t] = cin;
end

cin = overflow & cin;

logic [WIDTH-1:0] a, b;
logic [WIDTH-1:0] sum, overflow;

module adder #parameter WIDTH=3 (sum, overflow, a, b, cin);

assign overflow = carries[WIDTH-1] & carries[WIDTH-2];
assign cin[0] = cin;
endmodule
Advanced Verilog – "II” Synthesis