What components are on your DE1-SoC board, and how are they connected?
Advanced Verilog – Synthesizes Optimizations
module
  [\text{\texttt{carries[0] = carry}};
  \text{\texttt{assign over\texttt{flow} = carries[\text{\texttt{MIDTH-1}}]}}
endmodule
Advanced Verilog - "If" Synthesis