\[ c = \bar{a} \times (d + e) \]
\[ b = a \oplus d \]

draw the circuit it represents.

Is the following good Verilog? If not, fix it. If so, always comp begin

logic a, b, c, d, e;

begin
    if (a)
        c = d | e;
    else
        b = d;
        \( \bar{c} \)
        if (c = 0)
            p = 0;
end

Review Problem 56
end
case (ps)
  always_comb begin
    Next State Logic
    logic [1:0] us, ps;
    parameter [1:0] A = 2'b00, B = 2'b01, C = 2'b10;
    input w;

Advanced Verilog - "Case" Synthesizes
Advanced Verilog - "Posedge Statements"

end

else

ps => start;

if (reset)

always @ (posedge clk) begin

parameter [1:0] start = 2'b01;

logic [1:0] ps, ns;

Advanced Verilog - Counters
Advanced Verilog - Histogram

always @ (posedge clk) begin
  case (tival)
    3'd0: if (count10 > count11) count10 = count10 + 4'd0001;
    3'd1: if (count10 > count11) count10 = count10 + 4'd0001;
    3'd2: if (count10 > count11) count10 = count10 + 4'd0001;
    3'd3: if (count10 > count11) count10 = count10 + 4'd0001;
  endcase
end

2'b11: count11 <= count11 + 4'b0001;
2'b10: count10 <= count10 + 4'b0001;
2'b01: count10 <= count10 + 4'b0001;
2'b00: count10 <= count10 + 4'b0001;