Write Verilog that would create this circuit.

Review Problem 57
Advanced Verilog - Less Than
Advanced Verilog – Sequential Statements

output logic [2:0] 00, 01;
input logic [2:0] 10, 11;

if (01 > 00) begin
    if (01 == 11) begin
        o0 = 11;
        o1 = 10;
    end
    o0 = 10;
end

always_comb begin
end

end

end
Advanced Verilog - For Loops
All circuit elements built from transistors

Readings: 1.7-1.7.7

CMOS Transistors
Good 1  
False 0

However:

open switch =

closed switch =

P-type

N-type

Transistor Switches

Bad at carrying the voltage

TRUE = 1.2 volts

FALSE = 0 volts

Inverted gates
Transmission Gate

Make a switch that transmits 0 and 1.