1.) Convert the following assembly language program to machine code. The code begins at address 100\textsubscript{10}. Your answer must be in binary in the spaces provided (CMP at top, ADDI at bottom).

\begin{verbatim}
CMP X1, X2
B.LT ELSEIF
ADDI X1, X3, #5
ELSEIF:
\end{verbatim}

Second copy if you need it – but if you use it, indicate which to grade!!!:

\begin{verbatim}
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
\end{verbatim}
2.) We are given a program that executes 6 adds, 4 branches, 6 loads, 2 store, and 2 subtracts. Our compiler can fill ½ the delay slots in this code. If the single-cycle has a clock cycle of 10ns, and the pipelined has a clock cycle of 3ns, how much time will each machine take to complete the program? Assume that all machines are built like those discussed in class.

Single-cycle takes _____ ns.

Pipelined takes _____ ns.
3.) Register X0 has the address of an array of positive integers in memory, while X1 has the length (and is at least 5, perhaps longer). In assembly, write a program that will set X15 to the maximum value in that array. Your program should be as simple and efficient as possible. It should be written for a normal (non-pipelined) CPU. You can modify the value in any of the registers, including X0 and X1.
4.) We wish to add the instruction “BNEZ_R” – Branch to register if not equal to 0 – to the single-cycle processor from class. It is like a BR instruction, except it will NOT branch if the address is 0. The RTL for this instruction is given below:

```
Instruction = Mem[PC];
Cond = (true if Reg[Rd] != 0);
if (Cond) PC = Reg[rd];
else PC = PC + 4;
```

Show any modifications to the datapath necessary to accommodate this instruction. You should try to modify the datapath as little as possible. Then, on the next page list the control setting for the BNEZ_R instruction (only).
Control settings:

<table>
<thead>
<tr>
<th></th>
<th>BNEZ_R Control Setting:</th>
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</thead>
<tbody>
<tr>
<td>Reg2Loc</td>
<td></td>
</tr>
<tr>
<td>ALUSrc</td>
<td></td>
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<tr>
<td>MemToReg</td>
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<tr>
<td>RegWrite</td>
<td></td>
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<tr>
<td>MemWrite</td>
<td></td>
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<tr>
<td>BrTaken</td>
<td></td>
</tr>
<tr>
<td>UncondBr</td>
<td></td>
</tr>
<tr>
<td>ALUOp</td>
<td></td>
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</tbody>
</table>
5.) Create a single-cycle processor that can do “SUB” and “BR” only. Draw the \textit{datapath} for this machine (including the internals of the instruction fetch unit). Note that your machine should be as simple as possible.

Datapath: