For all of the questions in this homework, consider the pipelined CPU discussed in class, which is similar to the CPU in lab #4. That is, it has branch and load delay slots, forwarding logic from class (NOT the book), and accelerated branches.

1.) For the following code, explain what is happening in each stage of the pipelined processor during cycle 5.

   ```
   ADDI X0, X31, #102
   LDUR X1, [X0, #10]
   STUR X0, [X0, #10]
   CBZ X1, LOOP
   EOR X6, X4, X1
   ```

2.) Our processor has a load delay slot, which means code cannot use the Rd register of a load in the instruction right after a load. What happens if we ignore this restriction? Specifically, assume the following code is given to the CPU. Assume MEM[24] = -12. What value will end up in register X5? Think carefully – this one is tricky!

   ```
   ADDI X3, X31, #16
   LDUR X3, [X3, #8]
   ADD X5, X3, X3
   ```

3.) The following code contains a “read after write” data hazard that is resolved by forwarding:

   ```
   ADD X2, X3, X4
   ADD X5, X2, X6
   ```

   Consider the following code where a memory read occurs after a memory write:

   ```
   STUR X7, [X2, #100]
   LDUR X8, [X2, #100]
   ```

   Does the code work correctly? Why/why not? Will the forwarding unit need to be altered to handle this code?

4.) Consider a processor with the follow delays in each of the individual units:

<table>
<thead>
<tr>
<th>IF</th>
<th>ID</th>
<th>EX</th>
<th>MEM</th>
<th>WB</th>
</tr>
</thead>
<tbody>
<tr>
<td>200ps</td>
<td>150ps</td>
<td>120ps</td>
<td>190ps</td>
<td>140ps</td>
</tr>
</tbody>
</table>

   a.) What is the clock cycle time in a pipelined and non-pipelined processor?

   b.) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split, and what is the new clock cycle time of the processor?
5.) For the following code, explain what the register file and forwarding unit are doing during the fifth cycle of execution. If any comparisons are being made, mention them. Remember, use the forwarding unit from class, not the book.

```
LOOP:
  LDUR  X1, [X6, #40]
  ADD   X5, X5, X8
  ADD   X6, X6, X8
  STUR  X1, [X5, #20]
  CBZ   X1, LOOP
```