1.) For the code below draw the constraint graph. Label each edge with the cause of the constraint (i.e “RAW X2”, etc.).

```assembly
LOOP:
    LDUR X1, [X6, #40]
    ADD X5, X5, X1
    STUR X1, [X5, #20]
    ADDI X6, X6, #4
    SUBI X5, X5, #4
    CBZ X5, LOOP
```

2.) For the code below draw the constraint graph. Then adjust the code to run as fast as possible on a pipelined processor like that in lab #4. Note that if you carefully adjust the program you should be able to fill all the delay slots of the program (tricky! Think outside the box).

```assembly
LOOP:
    LDUR X2, [X10, #0]
    SUB X4, X2, X3
    STUR X4, [X10, #0]
    LDUR X5, [X10, #8]
    SUB X6, X5, X3
    STUR X6, [X10, #8]
    ADDI X10, X10, #16
    CMP X10, X30
    B.NE LOOP
```