Design a single-cycle CPU that can execute

SUBS and B.GE instructions only.
What should be done to this code to run it on a CPU with delay slots?

Noops? Legal, but not the best.

Both Reads

LDUR

STUR

XO, [x3, #17]

x1, x3, xo

SUBS

B.LT

ADDI

x3, x1, #8

LDURB

XO, [XH, #0]

Fclass

SUBS

x1, x3, xo

COPY

5x2

ADDE

uses x6, ADDE

Class not
Write a set of ARM assembly instructions that can accomplish the task of the given pseudo-instruction. You may use only register X7.

LONGB AddrImm64
Unconditionally branches to the 64-bit immediate address AddrImm64.

B AddrImm64  Too big a constant!

MOV2 X7, AddrImm64[15:0] LSL 0
MOVK X7, AddrImm64[31:16] LSL 16
MOVK X7  [47:32] LSL 32
MOVK X7  [63:48] LSL 48
BR X7
Convert the following to machine code:

```
LDRR X2, L#1, #47
LSL X1, X1, #3
```

Loop: 

```
ADDI X1, X31, #10
```

Loop:

B Loop

EE464 Homework 5A
Translate the following Java code to ARM assembly code. Assume sum, i, and registers x0, x1, respectively.

```java
int sum = 0;
for (int i = 0; i < 10; ++i) {
    if (i % 2 == 0) {
        sum += i;
    }
}
```
of 2 seconds, what is the minimum clock rate?

the same machine. If we would like the machine to run both X and Y in a total

(b) Assume that the program Y has \(3.5 \times 10^9\) instructions with a CPI of 2.5 on

(a) What is the expected CPU execution time for the program X?

2.5 \times 10^9\) instructions and a CPI of 1.5.

Suppose we have a 3.0 GHz machine that will run the program X with
the first integer of the array in memory is at register X0.
array into register X1 by using a loop implementation. The address of
Write a set of assembly code that puts the max value of a 10-integer
HW5a Question:
\[ PC = PC + 4 \]
\[ RA = (Rn, \text{SHAMT}) + PC \]
\[ PC = \text{M[PC]} \]
\[ LSLA Rk, Rn, \text{SHAMT} \]
\[ RSC \quad Rk, Rn, \text{SHAMT} \]
\[ RFSRd = \text{RegExReg} + \text{Reg[SHAMT]} \]
\[ PC = \text{M[PC]} \]
\[ \text{When in structure \text{Reg} = \text{Rm'}} \]
\[ \text{Ack Rk, Rn, SHAM} \]
\[ PC = \text{Reg[SHAMT]} \]
\[ R - \text{Reg} \]

Self Processors Data Path.
STUR X1, [X4, #10]
ADD X4, X5, X6
CBZ X4, LOOP
SUBI X4, X3, X31
ADD X3, X1, X2
ADD X31, X1, X1
LDRR X1, [X0, #10]

CYCLE

3) List the forwarding logics and their # of clock

using delay slot or no-op

2) If instructions need revise, please give solution

1) If any hazards exist, list and explain them.

Answer questions below:

Considering the following instructions, please
A single cycle CPU runs a program with a billion instructions in exactly 2 seconds. How fast will this program run on a pipelined CPU with a clock speed 10x as fast? Assume the program contains 10% loads and 10% branches, and the delay slots for these instructions are filled half the time.
intermediate storage

register X16 for

ADD. You may only use

LDR, STUR, AND and

LDRB, STURB, AND and

in terms of \[ \text{Imm9} \]

STURB, Rd, [Rn, \text{Imm9}]

and

Implementation LDRB, Rd,
\[\text{uncond} = 1, \text{ALUOp} = X, \text{MemWrite} = 0, \text{BRTaken} = 1, \text{MemToReg} = X, \text{RegWrite} = 0, \text{RegToReg} = X, \text{ALUsrc} = X, \text{PCrelLoc} = X, \text{ALUOp} = +\]

accomplish.

CPU could be trying to

instruction(s) that the

determine the

below, determine the

Given the control signals
RegFile: Stores the address of the next instruction into both the Data Memory and Instruction Memory. Command 19 Modify the datapath such that it can execute the following instruction. Also determine what values the control signals must be to execute the Instruction.
Does the following set of instructions lead to any pipeline hazards, if so, which hazards and where do these issues arise in the instruction set? How does the pipelining system rectify these issues?

LDUR \( X_0, [x_1, #0] \)
ADDI \( X_1, X_3, X_5 \)
CBZ \( X_2, X_3, X_4 \)
SUB \( X_4, X_3, X_6 \)
AND \( X_6, X_3, X_6 \)

END: