64-bit sign-extend unit that can handle both extended, while others are not. Build a 16-bit to immediate vals for some instructions are sign-
Store Instruction: Store Rd, [Rn, Addx9]

\[ R_c = R_c + 4 \]

\[ \text{MoveAddr = Reg Addr} \]

\[ \text{Addx = RegAddr + SE (Addr9)} \]

\[ \text{Instruction = Memory} \]
Datapath + Store

Adder = (Reg [specific address] + Shift) + 1

MEM[address] = Key (READ);

REG[address] = Key (READ);
Branch Instruction: B BRADDR26

If branch = MEMPCY:

PC = PC + 5E(B, ADD26) << 2;

// Instruction = MEMPCY;

PC = PE + 4D. ADD26 << 2;

If branch = MEMPCY:

PC = PC + 4D. ADD26 << 2;

If branch = MEMPCY:
Datapath + Branch
<table>
<thead>
<tr>
<th>Rd</th>
<th>CondAdd19</th>
<th>Opcode</th>
</tr>
</thead>
</table>

- $p_c = p_c + 4$
- If (cond) (if cond)
  - 75 ($\text{REG[15]} = p_c$)
  - $\text{REG[15]} = 0$
- Instruction = MEA LPC
  - Conditional Branch Instruction: CBE Rd, CondAdd19