Control settings for the NOP instruction. What are the NOP (no operation) function? To allow a CPU to spend a cycle waiting, we use a

Review Problem 26
Advanced: Exceptions

I/O device request (called an "interrupt")

Hardware failure

Call an undefined instruction

Arithmetic overflow, divide by zero,

... Exception = unusual event in processor

Save state (Exception Program Counter), protect the CPR, note cause

Have hardware detect these events & react:
Performance of Single-Cycle Machine
Reducing Cycle Time

Do same work in two fast cycles, rather than one slow one.
Cut combinational dependency graphs and insert registers / latches.
"Folder" takes 20 minutes
Dryer takes 40 minutes
Washer takes 30 minutes

Each have one load of clothes to wash, dry, and fold.

Ann, Brian, Cathy, & Dave

Example: Doing the Laundry

Readings: 4.5-4.8
Sequential laundry takes 6 hours for 4 loads. If they learned pipeline, how long would laundry take?
Pipelined Laundry takes 3.5 hours for 4 loads

Order

Task

Time

6 PM 7 8 9 10 11 Midnight

Pipelined Laundry: Start work ASAP
Pipeline Lessons

- Pipeline rate limited by slowest stage or entire workload throughput.
- Single task, it helps latency of pipeline doesn't help.
- Potential speedup = Number of pipe stages
- Simultaneously using different tasks operating pipeline stage.
- Pipeline reduces speedup.
- Unbalanced lengths of pipe stages.
- Time to "fill" pipeline and time to drain it reduces speedup.
- Stall for dependencies.
Now we just have to make it work.
Suppose we execute 100 instructions

Ideal Pipeined Machine

\[ \frac{10 \text{ ns/cycle}}{1 \text{ CPI x 100 inst + 4 cycle drain}} = 1,040 \text{ ns} \]

Single Cycle Machine

\[ \frac{45 \text{ ns/cycle}}{1 \text{ CPI x 100 inst}} = 450 \text{ ns} \]
CPI = 1.5 \\

\[ \frac{0.6 \times 60\%}{1} = 0.3 \]

Others \[ 0.6 \times 2 \times 30\% = 0.3 \]

Loop \[ 3 \times 10\% = 0.3 \]

Branches and 30% loads. What is the CPI on this program?

Example: A processor wastes 2 cycles after every branch, and 1 after every load, during which it cannot issue a new instruction. If a program has 10% load, 20% branches, and 40% other instructions, what is the CPI?

CPI in pipelined processor is "issue rate." Ignore fill/drain. Ignore latency.

\[ 10 \text{ ns/cycle} \times (1 \text{ CPI} \times 100 \text{ inst} + 4 \text{ cycle drain}) = \text{ns} \]

Ideal pipelined machine CPI for pipelined processors.