5th cycle of a pipelined CPU running this code?

What registers are being read and written in the

Review Problem 31
Cycle 1

Wait 1/2 cycle per
A/C branch?

Assume 50% branches

ADD x1, x2, x0
...
ADD x3, x3, x3

Compiler/Assembler fills the delay slot

Instruction after branch is the delay slot

Redefine branches: Instruction directly after branch always executed

Solution #3: Branch Delay Slot
Data Hazards

Consider the following code:

0 OR 9, X0, X10
8 ORR X7, X0, X8
6 AND X5, X0, X6
4 SUB X3, X0, X4
2 ADD X0, X1, X2

123
Design Register File Carefully

What if reads see value after write during the same cycle?

Instruction Set:
- ORR
- AND
- SUB
- ADD

Cycle Times:
- Cycle 1
- Cycle 2
- Cycle 3
- Cycle 4
- Cycle 5
- Cycle 6
- Cycle 7
- Cycle 8
- Cycle 9
Forward the ALU output to later instructions

Add logic to pass last two values from ALU output to ALU input(s) as needed
Compare sources of current instruction to destinations of previous 2.
Remember destination register for operation.
Requires values from last two ALU operations.