What forwarding happens on the following code?

Review Problem 34
Data Hazards on Loads (cont.)

Solution:

Force compiler to not allow register reads within a cycle of load.

Use same forwarding hardware & register file for hazards. 2+ cycles later

Fill delay slot or insert no-op.
\[
\text{Single cycle: CPI = 1.0, cycle time = 4.5 ns.} \\
\text{Delay for 1M instr.} \\
\text{Pipeline: cycle time = 1 ns.}
\]

\[
\begin{array}{|c|c|c|c|}
\hline
\text{CPI} & \text{Type Frequency} & \text{Type Cycles} & \text{Instruction Type} \\
\hline
1.2 & \text{Branch} & 1.5 & \text{Branch} \\
0.3 & \text{Store} & 1.5 & \text{Store} \\
0.1 & \text{Load} & 0.5 & \text{Load} \\
0.5 & \text{ALU} & 0.5 & \text{ALU} \\
\hline
\end{array}
\]

CPI: Assuming compiler can fill 50% of delay slots

Pipelined CPI, cycle time

\[
N = \frac{1}{\text{CPI}} = \frac{1}{1.2} = 0.8333
\]
Concerns:

- Comprehend cycle time by observing.
- Trace cycle time by observing.
- Объяснить времена переключения.
- Time = Initial Timer + Time 1 + Time 2 + Time 3

Pipelined CPU Summary

- Accelerated Branches
- Forwarding

Concerns:

- Comprehend cycle time by observing.
- Trace cycle time by observing.
- Объяснить времена переключения.
- Time = Initial Timer + Time 1 + Time 2 + Time 3

Assume PC is in the background.

Context: Page title: Pipeline CPU Summary