Review Problem 50

- For the constraint graph for this SWAP code, is there an edge between the two SW’s?

1: LDUR X0, [X5, #0]
2: LDUR X1, [X6, #0]
3: STUR X1, [X5, #0]
4: STUR X0, [X6, #0]
Complex ILP Example

Note: Assume no delay slots.

1: LDUR X0, [X3, #0]
2: ADD X1, X0, X2
3: SUB X2, X3, X4
4: ANDI X2, X5, #57
5: ORR X7, X5, X1
6: STUR X5, [X9, #0]
7: CBZ X7, LOOP
8: EOR X6, X8, X6
<table>
<thead>
<tr>
<th>Local delay slot</th>
<th>1</th>
<th>1</th>
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<tbody>
<tr>
<td></td>
<td>6</td>
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<td>2</td>
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<td>3</td>
<td>5</td>
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<td>5</td>
<td>3</td>
</tr>
<tr>
<td>Branch delay slot</td>
<td>4</td>
<td>7</td>
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<tr>
<td></td>
<td>7</td>
<td>4</td>
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<td>8</td>
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Types of Hazards

Data Hazards (multiple uses of the same location)
- RAW – Read after write
- WAW – Write after write
- WAR – Write after read
- RAR – Read after read

Memory

Control Hazards
- Branches