Review Problem 53

- In assembly, replace the value in X0 with its absolute value, without using any branches.

```
SUBS  x1,x31,x0  // x1 = -x0
CSEL  x0, x0, x1, LE

LSR  x2, x0, #63
SUB  x2, x31, x0
CMOUNZ x0, x1, x2
```
Why ILP

Advanced processors optimize two factors:

- Reduce clock period by heavy pipelining
  Greater pipelining means more hazards, delay slots

- Reduce CPI
  What if we want a CPI < 1.0?
Superpipelining

Divide datapath into multiple pipeline stages

Pentium 4 Processor ("NetBurst"): 20 stages

<table>
<thead>
<tr>
<th>TC</th>
<th>Nxt IP</th>
<th>TC Fetch</th>
<th>Decode</th>
<th>Alloc</th>
<th>Rename</th>
<th>Queue</th>
<th>Schedule</th>
<th>Dispatch</th>
<th>Reg File</th>
<th>Exec</th>
<th>Flags</th>
<th>Brnch</th>
<th>Ck</th>
<th>Drive</th>
</tr>
</thead>
</table>

- Update PC in Fetch
- Instructions in register
- Solving the constraint
- ALU execution
- Branch prediction
- Remaining
Multiple Issue

Replicate Execution Units

PC \rightarrow \text{Instr. Memory} \rightarrow \text{Register File} \rightarrow \text{Data Memory} \rightarrow \text{Register File}

ALU
Shifter
Floating Point
Register File: Many Ports
Memory: Only Affected One
Ifetch/Branch

4 Instructions/Cycle
**VLIW**

Very Long Instruction Word

<table>
<thead>
<tr>
<th>ALU</th>
<th>ALU</th>
<th>Load/Store</th>
<th>Branch</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="ALU symbol" /></td>
<td><img src="image2" alt="ALU symbol" /></td>
<td><img src="image3" alt="Load/Store symbol" /></td>
<td><img src="image4" alt="Branch symbol" /></td>
</tr>
</tbody>
</table>

Max CPI?

0.25

Concerns

- Waste instruction memory if lots of loops.
- Simple HW. Complex compiler.
- Code compatibility → None

VLIW is for DSP.
VLIW Scheduling

Schedule the code for a 4-way VLIW. Assume no delay slots, and all instructions in parallel with a branch still execute.

1: LDUR X6, [X0, #4]
2: ADD X7, X6, X0
3: LDUR X8, [X1, #8]
4: SUB X7, X8, X2
5: STUR X10, [X3, #0]
6: CBZ X4, FOO
7: AND X12, X4, X5

<table>
<thead>
<tr>
<th>ALU1</th>
<th>ALU2</th>
<th>Load/Store</th>
<th>Branch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noop</td>
<td>Noop</td>
<td>1: LDUR</td>
<td>Noop</td>
</tr>
<tr>
<td>2: ADD</td>
<td>Noop</td>
<td>3: LDUR</td>
<td>Noop</td>
</tr>
<tr>
<td>Noop</td>
<td>4: SUB</td>
<td>5: STUR</td>
<td>G: CBZ</td>
</tr>
<tr>
<td>7: AND</td>
<td>Noop</td>
<td>Noop</td>
<td>Noop</td>
</tr>
</tbody>
</table>

\[ CPI = \frac{4}{7} = \frac{4}{7} \]